19. Japan Patent Office (JP)

12. Laid-open Patent Gazette (A)

11. Laid-open Patent Application No. Sho 60-80193

51.Int. Cl.[4]	ID No.	Office Control No.
G 11 C 7/00		6549-5B

43. Date Published: May 8, 1985

Examination Not Requested Yet

Number of Inventions: 1 (Total 5 pages in original)

54. Title of Invention: Memory System

21. Application Number: Sho 58-186919

22. Application Date: October 7, 1983

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SPECIFICATION

TITLE OF THE INVENTION

Memory System

CLAIMS

(1) A memory system, comprising a plurality of storage device blocks with different operating times, an address decoder that receives system address signals and detects access to said storage device blocks, a counting circuit that sets an initial value equivalent to the access time in the storage device block corresponding to the address decoder's output signal and that measures time using a specified pulse signal, and a timing control circuit that sets writing or reading operating time for the storage device block according to the counting circuit's output signal.

(2) The memory system set forth in claim 1, wherein said counting circuit comprises a shift register.

(3) The memory system set forth in claim 1 or claim 2, wherein said timing control circuit forms a timing signal that takes the read output signal into a latch circuit and an operation end signal sent to a central processing device.

DETAILED DESCRIPTION OF THE INVENTION

Technical Field

The present invention pertains to a memory system, for example, to a technique for effective timing control of a memory system comprising a storage device block using high-speed storage devices and a storage device block using low-speed storage devices.

Prior Art

For example, if a single memory system comprises a plurality of storage device blocks with different operating times, such as high-speed RAM (random access memory), low-speed RAM, or ROM (read only memory), the operating time is different for each storage device block, so the following sorts of problems occur in timing control thereof. If all of the storage device blocks are controlled with a single timing, all of the storage device blocks are operated according to the timing of the slowest storage device block. On the other hand, if each storage device block is accessed with the optimal timing by providing them with individual timing generation circuits, this leads to the problem that timing control circuit becomes complex and the number of constituent components increases.

Object of the Invention

The object of the present invention is to provide a memory system that can access a plurality of storage device blocks with different operating speeds based on their respective optimal timing by means of a simple constitution.

The aforesaid and other objects of the present invention and its novel features shall become clear from the description in this specification and from the drawings.

Summary of the Invention

Of the inventions disclosed in this application, a summary of a representative one can be simply explained as follows. That is, it receives a system address signal and detects access to storage device blocks with different operating speeds, and sets an initial value equivalent to the access time in the storage device block corresponding to the output signal, and sets the writing or reading time for each storage device block according to the output signal from a counting circuit which measures time using a specified pulse signal.

Working Example

FIG. 1 is a block diagram of one working example of the present invention. The memory system in this working example is not particularly restricted, but the example described is one that uses two types of storage devices: high-speed storage device 6 and low-speed storage device 7.

In this working example, timing control of the aforesaid storage devices 6 and 7 is performed by a timing control circuit as follows. That is, access to one of two types of memory device 6 or 7 is detected by address decoder 1 receiving a system address signal from address bus AB. This detection output m1 and m2 is used as selection signals for selector 4. Selector 4 selects storage means 2 and 3, which are holding initial values T1 and T2, and supplies initial values T1 or T2 to shift register 5. Shift register 5 loads the aforesaid initial values T1 or T2 according to timing signal $\phi 1$ formed by the aforesaid address decoder 1. This is not particularly restricted, but shift register 5 comprises a 10-bit shift register. Output signal D7~D10, which is the seventh through tenth bits of shift register 5, is then supplied to a timing detection circuit constituted using the AND gate circuits G1~G4.

That is, seventh bit signal D7 is inverted by inverter circuit IV1, and is supplied with eighth bit signal D8 as input to AND gate circuit G4. AND gate circuit G4's output signal is used as a strobe signal for latch register 8, which receives read output signal D_{out} from storage device 6 or 7. The aforesaid address decoder 1's output signal m1 and shift register 5's eighth bit signal D8 are supplied as input to AND gate circuit G2. AND gate circuit G2's output signal CS1 is used as a chip selection signal for high-speed storage device 6. The aforesaid address decoder circuit 1's output signal m2 and shift register 5's eighth bit signal D8 are supplied as input to AND gate circuit G3. AND gate circuit G3's output signal CS2 is used as a chip selection signal for low-speed storage device 7. Also, shift register 5's ninth bit signal D9 is inverted by inverter circuit IV2 and is supplied with tenth bit signal D10 as input to AND gate circuit G1. AND gate circuit G1's output signal is used as operation end signal ACK sent to a central processing unit (CPU) not shown in the drawing.

Meanwhile, the storage device side controlled by the aforesaid timing control circuit is connected to data bus DB via bidirectional buffer 9, which is connected to storage devices 6 and 7's data input D_{in} and data output D_{out}, via the aforesaid latch

register 8. Furthermore, address signals are supplied to the storage devices 6 and 7 from address bus AB (not shown in drawing).

Next, the operation of the memory system in this working example shall be described according to the timing diagrams of FIG. 2 and FIG. 3.

FIG. 2 shows a timing diagram when accessing low-speed storage device 7 (M2). This working example is not particularly restricted, but 0111111100 is held in storage means 3 as its initial value T2. Therefore, when a system address signal to select storage device 7 is supplied to address decoder 1, its output signal m2 is formed, and via selector 4 the aforesaid initial value T2 is supplied to shift register 5. Then the aforesaid initial value T2 is taken into shift register 5 in sync with load signal $\phi 1$ formed by output signal m2 and clock ϕ. Therefore the seventh and eighth bit signals D7 and D8 become 1 per the timing of the first clock ϕ, and the remaining ninth and tenth bit signals D9 and D10 become 0. This sort of initial value T2 is sequentially shifted to the right, one bit at a time, according to clock ϕ. Signals D9 and D10 sequentially become 1, each delayed one clock by the shift operation. Also, when the seventh clock ϕ arrives, first bit 0 in initial value T2 is shifted to the seventh bit, so signal D7 becomes 0. Subsequently, signals D8~D10 also sequentially change to 0, each delayed by one clock.

Through the aforesaid shift operation of shift register 5, storage device 7 (M2) is selected by the output signal CS2 of AND gate circuit G3, which receives the aforesaid address decoder 1's output signal m2 selection signal (logical "1") and the aforesaid eighth bit signal D8. Then, when signal D7 changes to 0 (low level), strobe signal $\phi 2$ is formed, so if it's a read operation read signal D_{out} from storage device 7 is taken into latch register 8. In addition, signal D9, delayed by two clocks, becomes 0, so the operation end signal ACK is sent by AND gate circuit G1 and access ends. That is, central processing unit CPU not shown in the drawing receives the aforesaid operation end signal ACK, and receives the aforesaid read data D_{out}, via the bidirectional buffer. Furthermore, if it's a write operation, input data D_{in} is supplied to storage device 7 during the aforesaid chip selection interval CS2, and [the CPU] waits for transfer of operation end signal ACK in the same manner as noted above to end the operation.

FIG. 3 is a timing diagram when accessing high-speed storage device 6 (M1). This working example is not particularly restricted, but 0000011100 is held in storage means 2 as its initial value T1. Therefore, when a system address signal to select storage device 6 is supplied to address decoder 1, its output signal m1 is formed, and via selector 4 the aforesaid initial value T1 is supplied to shift register 5. Then the aforesaid initial value T1 is taken into shift register 5 in sync with load signal $\phi 1$ formed by output signal m1 and clock ϕ. Therefore the seventh and eighth bit signals D7 and D8 become 1 per the timing of the first clock ϕ, and the remaining ninth and tenth bit signals D9 and D10 become 0. This sort of initial value T1 is sequentially shifted to the right, one bit at a time, according to clock ϕ. Signals D9 and D10 sequentially become 1, each delayed one clock by the shift operation. Also, when the third clock ϕ arrives, fifth bit 0 in initial value T1 is shifted to the seventh bit, so signal D7 becomes 0. Subsequently, signals D8~D10 also sequentially change to 0, each delayed by one clock.

Through the aforesaid shift operation of shift register 5, storage device 6 (M1) is selected by the output signal CS1 of AND gate circuit G3, which receives the aforesaid

address decoder circuit 1's output signal m1 selection signal (logical "1") and the aforesaid eighth bit signal D8. Then, when signal D7 changes to 0 (low level), strobe signal $\phi 2$ is formed, so if it's a read operation read signal D_{out} from storage device 6 is taken into latch register 8. In addition, signal D9, delayed by two clocks, becomes 0, so the operation end signal ACK is sent by AND gate circuit G1 and access ends. That is, central processing unit CPU not shown in the drawing receives the aforesaid operation end signal ACK, and receives the aforesaid read data D_{out}, via the bidirectional buffer. Furthermore, if it's a write operation, input data D_{in} is supplied to storage device 6 during the aforesaid chip selection interval CS1, and [the CPU] waits for transfer of operation end signal ACK in the same manner as noted above to end the operation.

Through the aforesaid operation low-speed storage device 7 operates for an interval of seven clocks ϕ, and high-speed storage device 6 operates for an interval of three clocks ϕ. Therefore in this working example the memory device operating time can be made consistent using one cycle of the aforesaid clock ϕ and the number of clocks. Setting this sort of operating time (access time) is easy to do by setting the aforesaid initial value.

Effect

(1) Using a single timing control circuit comprising simple circuits such as an address decoder, shift register, selector, and gate circuit, it is possible to obtain a memory system, comprising a plurality of storage devices with different operating times, that can operate based on cycles corresponding to the operating time for each storage device.

(2) Timing can be controlled using simple circuits as in (1) above, so the failure rate of the overall memory system can be reduced.

(3) The number of constituent components of the timing control circuit is reduced as in (1) above, so it is possible to obtain an inexpensive memory system.

(4) Each storage device can be accessed at its optimal operating cycle by using (1) above, so there are no inefficiencies in memory access. Therefore it is possible to rationalize storage information input and output.

The invention created by the inventors was described in specifics based on the working example presented above, but the present invention is in no way restricted to the aforesaid working example; various modifications can be practiced without departing from its essence. For example, timing can be controlled for three or more types of storage devices according to their respective operating times in the same manner as noted above by adding storage means for holding the aforesaid initial values and gate circuits. Also, a time measuring (pulse counting) circuit such as a programmable counter or the like may be used as the circuit that sets time according to the operating time of each storage device instead of the aforesaid shift register.

In addition, the structure of the specific circuits of each circuit block can take various configurations.

Field of Utilization

The present invention is widely used in memory systems comprising a plurality of storage devices with different operating speeds.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing one working example of a memory system in accordance with the present invention.

FIG. 2 is a timing diagram for explaining timing control of a low-speed storage device.

FIG. 3 is a timing diagram for explaining timing control of a high-speed storage device.

1	Address decoder
2,3	Storage means
4	Selector
5	Shift register
6	High-speed storage device
7	Low-speed storage device
8	Latch register
9	Bidirectional buffer

Agent: Akio Takahashi, patent agent [seal]

FIG. 1

1	Decoder
4	Selector
5	Shift register
6	High-speed memory
7	Low-speed memory
8	Buffer

FIG. 2

FIG. 3

(19) Japan Patent Office (JP)

(12) Laid-open Patent Gazette (A)

(11) Laid-open Patent Application Sho 60-55459

(43) Date Published: March 30, 1985

(51) Int. Cl.[4]	ID No.	Office Control No.
G 06 F 13/16		6974-5B
12/02		6974-5B
12/08		8219-5B

Examination Request: Not Requested

Number of Inventions: 1 (Total 10 pages in original)

(54) Title of Invention: **Block Data Transfer and Storage Control Method**

(21) Application Number: Sho 58-163161

(22) Application Date: September 7, 1983

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SPECIFICATION

TITLE OF THE INVENTION

Block Data Transfer and Storage Control Method

CLAIMS

1. A block data transfer and storage control method in a processing device structured so that the main processing device or input/output processing device, as the access origin, accesses the (main) memory via a memory control device,

wherein, when a request occurs at the access origin to transfer and store block data present at a nonspecific transfer origin memory area to a nonspecific transfer destination memory area that is another memory area within the same memory,

the access source transfers the transfer origin and transfer destination memory area starting addresses or ending addresses to the memory control device as transfer origin and transfer destination addresses, together with address update mode information and number of words to transfer, according to a decision on the size relationship between the transfer origin and transfer destination memory area addresses;

and the control device updates the transfer origin and transfer destination addresses, each time read data is transferred and stored from the transfer origin memory area to the transfer destination memory area, in the direction specified by said address update mode information, until the number of transfers and storages matches said number of words to transfer;

thereby controlling transfer and storage of block data from the transfer origin memory area to the transfer destination memory area.

2. The block data transfer and storage control method of claim 1 wherein, when memory access by the main processing device is performed via a cache memory, the cache memory compares and monitors each address in the (main) memory corresponding to data stored in itself and transfer destination addresses from the memory control device while transfer and storage are being performed, and if address matching is detected, data corresponding to that address is treated as invalid.

DETAILED DESCRIPTION OF THE INVENTION

Application Field of the Invention

The present invention pertains to a block data transfer and storage control method that transfers and stores block data stored in a memory area to another memory area within the same memory at high speed.

Invention's Background

It is often necessary to transfer and store block data stored in a certain memory area to another memory area within the same memory, but at present this transfer and storage cannot be done at high speed. What is referred to as block data transfer and storage is ordinarily, as shown in FIG. 1, in a case in which a data group having some sort of relationship continuously from address A to address B in memory 1 is stored as block data, the storage of that block data from address A' to address B' at another

memory area in a specified address sequence. Data at address A is transferred to and stored at address A', and that at address B respectively is transferred to and stored at address B'. This sort of block data transfer and storage is necessary in various types of processing fields, and its necessity is particularly high in fields such as text processing, phone terminal processing, CAD (Computer Aided Design), file management, etc. For example, when performing corrections on the display screen in a display device such as a CRT or the like, particularly when inserting or deleting a line or changing its position, the transfer and storage of about 80 bytes of block data frequently occurs.

FIG. 2 is a drawing showing the general overall structure of a processing device in accordance with the premises of the present invention.

According to this, (main) memory (main storage device) 1 stores programs and data, so a plurality of memory 1 is provided in order to improve throughput through interleaving. Control of writing to memory 1 or reading from memory 1 is performed by memory control device 2 via memory bus 6. Memory control device 2 is connected to bus 7; also connected to bus 7 are input/output processing device 5, and main processing device 4, which is connected via cache memory 3. In response to a memory read request from main processing device 4, cache memory 3 decides whether or not it stores within itself data related to that request, and if [that data] is stored within itself it reads that data from within itself and immediately transfers it to main processing device 4. If [that data] is not stored within itself, that data is read from memory 1 via memory control device 2, and then transferred to main processing device 4, and simultaneously stored within itself. Also, in response to a memory write request from main processing device 4, if data related to that write address is stored within itself, cache memory 3 rewrites and changes the data at that write address to the write data, and regardless of whether it is stored or not writes that data to memory 1 via memory control device 2. In addition, cache memory 3 monitors address signals transferred from input/output processing device 5 to memory control device 2, and if data at the address that is written to is stored within itself, that data is invalidated.

The following sorts of methods are known for performing high-speed block data transfer and storage in this sort of processing device.

That is, a first method is to transfer and store, from the access origin (main processing device 4) to memory control device 2, the transfer origin address, transfer destination address, and number of words to transfer, and subsequently memory control device 2 continues to update these addresses in the direction of increase, and to decrease the number of words to transfer, and to perform block data transfer and storage. Nevertheless, in this method block data transfer and storage is performed in the direction in which both the transfer origin address and the transfer destination address increase, so [there is no problem] if no parts of the transfer origin memory area and the transfer destination memory area overlap, but if they overlap failures occur. For example, in the case shown in FIG. 3, in which parts of the transfer origin memory area (addresses A~B) and the transfer destination memory area (addresses A'~B') overlap, if an attempt is made to transfer and store data at address A at address A', the contents of data at address A' are completely changed even though it is within the transfer origin memory area and should be transferred and stored later. Also, in this method transfer and storage processing is executed only between memory 1 and memory control device 2, so even if

data at addresses included in the transfer destination memory area is stored in cache memory 3 before transfer and storage, cache memory 3 is unable to perform any processing during transfer and storage, so it is clear that after transfer and storage the memory 1 data in cache memory 3 and the data in memory 1 do not agree.

A second method is to implement a simultaneous processing function in main processing device 4, and to sequentially read from the transfer origin memory area the data to be transferred by interleaving from memory 1, and to delay the read data for a certain time and then write it to memory 1 by interleaving. Starting reading and writing and updating addresses in this method is guided by main processing device 4, and the read data is transferred toward memory 1 as write data via main processing device 4, but when block data transfer and storage is performed in this manner the block data transfer speed is determined by the data transfer route unit with the lowest throughput. Generally speaking, in processing devices that seek high-speed processing the throughput of memory 1 itself is usually at least twice as high as data transfer between main processing device 4 and memory 1, but with this method it is not possible to achieve that high throughput.

Finally, a third method that has been contemplated is to not transfer data at input/output processing device 5 only between memory 1 and the input/output device, but rather to perform data transfer within memory 1 and lessen the load on main processing device 4. Nevertheless, with this method input/output processing device 5 increments the transfer origin and transfer destination addresses and performs block data transfer and storage while updating the addresses, so memory area overlaps produce the same sort of failures as in the first method. Also, with this method input/output processing device 5 receives instructions from main processing device 4 and controls and executes transfer and storage, but if the data being transferred is small (a few tens of bytes or so) data transfer and storage comes to a complete halt until main processing device 4 switches to and executes another program, and accelerating data transfer and storage cannot be achieved.

Object of the Invention

The object of the present invention is to provide a block data transfer and storage control method that transfers and stores block data stored at a certain memory area to another memory area in the same memory at high speed even if parts of the memory areas overlap, regardless of the overlap configuration, and without imposing a burden on the access origin.

Summary of Invention

In order to achieve this object, the present invention is constituted so that when the memory control device receives the transfer origin address and the transfer destination address as a memory area starting address or ending address from the access origin, number of words to transfer, and address update mode information, block data is transferred and stored within the same memory in a way such that the transfer origin and the transfer destination addresses are updated in the direction corresponding to the address update mode information. If the transfer origin starting address at the access origin is larger than the transfer destination starting address, the transfer origin starting address and the transfer destination starting address are transferred to the memory control

device as the transfer origin and transfer destination addresses, and increasing specification mode is transferred as the address update mode information. On the other hand, in the opposite situation the transfer origin ending address and the transfer destination ending address are transferred to the memory control device from the access origin as the transfer origin and transfer destination addresses, and decreasing specification mode is transferred as the address update mode information.

Working Examples of the Invention

Next, the present invention shall be explained using FIG. 4 through FIG. 11.

FIG. 4 schematically shows a cache memory and memory with the main functions of a memory control device in accordance with the present invention. Transfer origin address, transfer destination address, number of words to transfer, and address update mode information from cache memory 3 or input/output processing device [5] as the access origin are provided to memory control device 2 via bus 7, and then set in transfer origin address counter 202, transfer destination address counter 203, and address update mode specification register (1 bit) 201. This is not shown in the drawing, but the number of words to transfer is set in a separately provided remaining number of words to transfer counter. Then the count modes of counters 202 and 203 are specified by register 201, and if counters 202 and 203 are updated after data is read in address units from the transfer origin memory area in memory 1—that is, each time that data is written to the transfer destination memory area—block data in the transfer origin memory area is transferred to the transfer destination memory area at high speed and stored there. The counter for the remaining number of words to transfer, which is set with number of words to transfer, is decremented each time data is transferred and stored, and when that count value reaches zero, transfer and storage ends. Incidentally, when transfer and storage is performed, the contents of the data at the transfer destination memory area change and are different after transfer and storage than before, so failures occur if cache memory 3 is storing data included in the transfer destination memory area. Japanese Patent Application No. Sho 57-122153 discloses invalidation mechanism 31 in cache memory 3; the occurrence of this sort of problem can be prevented by using this to monitor addresses from counter 203. That is, it monitors and compares each address in memory 1 corresponding to data stored within itself and addresses from counter 203, and if it detects an address match the data corresponding to that address is treated as invalid.

FIG. 5 shows the specific structure of one example of that memory control device. According to this, the memory control device has bus occupancy selection circuit 205 related to bus occupancy control, and has function register 209, address register 208, write data register 207, read data register 211, and memory access control circuit 210 related to normal memory access control. In addition, it has the previously described transfer origin address counter 202, transfer destination address counter 203, remaining number of words to transfer counter 204, address update mode specification register 201, and additionally block data transfer control circuit 206 related to block data transfer. Furthermore, codes 212–222 in FIG. 5 indicate gates; their passage control is performed by memory access control circuit 210 or block data transfer control circuit 206.

Now, the operation of the aforesaid sort of memory control device shall be described as follows.

First, an ordinary memory read access operation is started by outputting bus occupancy request 234 from the cache memory or input/output processing device as the access origin to bus occupancy selection circuit 205. FIG. 6 shows major input/output signals and input/output data in the memory access operation. Bus occupancy request 234 is input to bus occupancy selection circuit 205 via a signal line corresponding to the access origin; bus occupancy requests 239 and 237 from memory access control circuit 210 and block data transfer control circuit 206 are also input to bus occupancy selection circuit 205. When bus occupancy selection circuit 205 has requests for bus occupancy, it selects one of them and then functions to provide bus occupancy permission. Bus occupancy permission 235 is given to the access origin, and bus occupancy permissions 238 and 236 are given to memory access control circuit 210 and block data transfer control circuit 206 respectively. FIG. 6 shows a case in which bus occupancy permission 235 is provided in response to bus occupancy request 234 from the access source.

The access source that receives bus occupancy permission 235 is started by it and can occupy the bus, and transfers function signal 231 and address signal 232. These signals are set in function register 209 and address register 208 in the memory control device; if the contents of function signal 231 are decoded by memory access control circuit 210 as memory read access, read mode memory function signal 241 and memory address signal 242 are provided to the memory. Meanwhile, the data read at the memory based on those signals is output as memory data 243 synchronized with memory response 240. Memory data 243 from the memory is temporarily set in read data register 211, and bus occupancy request 239 is output from memory access control circuit 210 to bus occupancy selection circuit 205 based on memory response 240. If the result of bus occupancy selection circuit 205's selection in response to this is to provide bus selection permission 238, memory access control circuit 210 outputs the contents of read data register 211 on the bus as data 233, and meanwhile outputs access origin identification information to the access origin as response 230. When the access origin detects that it itself has been specified by this access origin identification information, it starts taking data 233.

Ordinary read access to the memory is as described above, and ordinary write access too can be performed in the same way by this.

Next, block data transfer and storage shall be described. FIG. 7 focuses on the operation when this starts. This case includes the same sort of bus occupancy protocol as in ordinary memory access by the access origin; function signal 231 and data 233 from the access origin are respectively set in function register 209 and write data register 207. If block data transfer control circuit 206 decodes the contents of function register 209 and detects that it is a write request for the transfer origin address, the contents of write data register 207 are set in transfer destination address counter 202, and response 230 is transferred to the access origin. The access origin thereby next sets the transfer destination address in transfer destination address counter 203 in the same manner as above, and then sequentially sets the number of words to transfer and the address update mode information in remaining number of words to transfer counter 204 and address update mode specification register 201. In this case the number of words to transfer from the access origin and the address update mode information set request also function as a block data transfer and storage start request, so block data transfer control circuit 206

immediately starts block data transfer and storage after setting the number of words to transfer and address update mode information ends. Transfer and storage shall be explained in detail later, but when transfer and storage ends, response 230 to that effect is sent from block data transfer control circuit 206 back to the access origin. Therefore, the access source performs three continuous accesses in exactly the same manner as an ordinary write access, and then finishes simply by receiving a response to the effect that transfer and storage has ended, so high-speed transfer and storage of block data can be performed with little burden.

Now the relationship between the write data register and the remaining number of words to transfer counter and the address update mode specification register shall be explained using FIG. 8. Data 233 from the access origin is set as 32 bits, for example, but address update mode information and number of words to transfer are transferred simultaneously from the access origin in this example. In this, one bit suffices for the address update mode information, so the remaining 31 bits can be used for the number of words to transfer, but in this example one word is 32 bits and a maximum of 255 words can be transferred and stored at one time. Eight bits are assigned for the number of words to transfer, but it is not limited to this, of course.

Now, how transferring and storing block data is performed shall be explained using FIG. 9.

When address update mode information and number of words to transfer are set from the access origin, block data transfer control circuit 206 first outputs bus occupancy request 237 to bus occupancy selection circuit 205. If occupancy permission 236 is provided in response to this, next the contents of transfer destination address counter 203 are output as address signal 232; also output is function signal 231 indicating prior transfer and storage of the first data synchronized with this. Thereby the cache memory invalidates data when required using its cache invalidation mechanism. Meanwhile, in parallel with this, block data transfer control circuit 206 makes memory function signal 241 the read mode and outputs the contents of transfer origin address counter 202 to the memory as memory address signal 242, and thereby reads data corresponding to memory address signal 242 from the memory as memory data 243. In this case memory data 243 is read from memory and should be on the bus for a set time, so after response 240 is acquired, if memory function signal 241 is made the write mode and the contents of transfer destination address counter 203 are output as memory address signal 242, memory data 243 is transferred to and stored at the transfer destination memory area. Therefore, during the period until the contents of remaining number of words to transfer counter 204 become zero, the contents of remaining number of words to transfer counter 204 are decremented each time transfer and storage of one datum ends, and transfer origin and transfer destination address counters 202 and 203 undergo the specified updating, after which the aforesaid operation can be repeated.

FIG. 10 shows how address counters 202 and 203 are controlled by address update mode specification register 201. Address counters 202 and 203 are both reversible counters that can be reset, and whether they both count up or count down depends on the output status of the flip-flop that is address update mode specification register 201. The update direction of memory address signal 242 generated by address counters 202 and 203 is controlled according to set output 246 and reset output 245. This example is a case

of setting, controlled to count down. Furthermore, address update timing signal 247 is created by block data transfer control circuit 206 based on memory response 240 to accompany data transfer and storage.

Finally, the microprogram flow related to block data transfer and storage shall be explained. FIG. 11 shows the microprogram flow executed in the main processing device. In this case, first the bit pattern "000000FF" (hexadecimal notation) and the number of words to transfer (DC) undergo a logical product operation (AND), and the result is stored in temporary work register WK1. Here the maximum value for the number of words to transfer is "FF" (hexadecimal notation for each 4 bits), so it is necessary to first make the unspecified higher-order 24 bits "0". Next, the transfer origin and the transfer destination starting addresses are stored in temporary work registers WK2 and WK3 respectively, after which their size relationship is determined. According to the results of this decision, the transfer origin starting address and transfer destination starting address or the transfer origin ending address and transfer destination ending address are transferred to the memory control device as the transfer origin address and transfer destination address. If the transfer origin ending address and transfer destination ending address are transferred as the transfer origin address and transfer destination address, the contents of temporary work register WK1 undergo a logical sum operation (OR) with the bit pattern "80000000"; this is in order to make the address update mode information "F" into "1".

The present invention is as described above, and of course it can also be applied even if the transfer origin memory area and the transfer destination memory area completely match.

Effect of the Invention

The present invention, as described above, transfers and stores block data within the same memory by receiving transfer origin address, transfer destination address, number of words to transfer, and address update mode information from the access origin that generated a request for transfer and storage, and the memory control device updates the transfer origin and transfer destination addresses in the direction corresponding to the address update mode information. Therefore, the present invention has the effect that it transfers and stores block data stored at a certain memory area to another memory area in the same memory correctly and at high speed even if parts of the transfer origin memory area and the transfer destination memory area overlap, regardless of the overlap configuration, and without imposing on the access origin. In particular, it is possible to achieve high speed simply by making the data width between the memory and memory control device larger than in other parts, and data bus occupancy time on the memory bus for block data transfer is one-half of prior art, and decrease in throughput when transferring block data is reduced. The latest dynamic RAMs perform continuous address reading using nibble mode support (see *Nikkei Electronics*, April 1983), and the data bus load is large compared to the address bus load, so the present invention can have a great effect.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a drawing explaining ordinary block data transfer and storage within the same memory. FIG. 2 is a drawing showing the general overall structure of a processing

device in accordance with the premises of the present invention. FIG. 3 is a drawing explaining a failure when the transfer origin and transfer destination memory areas overlap. FIG. 4 is a drawing schematically showing the major functions in both cache memory and memory of a memory control device in accordance with the present invention. FIG. 5 is a drawing showing the specific structure of one example of a memory control device in accordance with the present invention. FIG. 6 is a drawing showing major I/O signals and I/O signal timing in order to explain the ordinary memory read access operation in that memory control device. FIG. 7 similarly is a drawing showing major I/O signals and I/O signal timing in order to explain the operation when a block data transfer and storage operation starts in that memory control device. FIG. 8 is a drawing showing the relationship between the write data register and the remaining number of words to transfer counter and the address update mode specification register in that memory control device. FIG. 9 is a drawing showing major I/O signals and I/O signal timing in order to explain a block data transfer and storage operation according to the present invention in a memory control device. FIG. 10 is a drawing for explaining how the transfer origin and transfer destination addresses are updated and controlled according to address update mode information. FIG. 11 is a drawing showing the microprogram flow related to the block data transfer and storage executed in the main processing device.

1... (main) memory (main storage device), 2... memory control device, 3... cache memory, 4... main processing device, 5... I/O processing device, 31... cache invalidation mechanism, 201... address update mode specification register, 202... transfer origin address counter, 203... transfer destination address counter, 204... remaining number of words to transfer counter, 205... bus occupancy selection circuit, 206... block data transfer and control circuit, 207... write data register, 208... address register, 209... function register.

Agent: Masami Akimoto, Patent Agent

FIG. 1

Address

FIG. 2

FIG. 3

Address

FIG. 4

Cache invalidation mechanism

FIG. 5

FIG. 6

Bus occupancy request 234

Bus occupancy permission 235

Function signal 231

Address signal 232

Data 233

Response 230

Memory function signal 241

Memory address signal 242

Memory data 243

Memory response 240

Bus occupancy request 239

Bus occupancy permission 238

FIG. 7

Bus occupancy request 234

Bus occupancy permission 235

Function signal 231

Address signal 232

Data 233

Response 230

Block data transfer

FIG. 8

FIG. 9

Bus occupancy request 237

Bus occupancy permission 236

Function signal 231

Address signal 232

Memory function signal 241

Memory address signal 242

Memory data 243

Memory response 240

FIG. 10

FIG. 11

First operand (number of transfer words)

Second operand (transfer origin starting address)

Third operand (transfer destination starting address)

Yes (Transfer from larger address)

No (Transfer from smaller address)

Wait for response

Wait for response

Wait for response

Wait for response

Wait for response

Wait for response

⑲ 日本国特許庁（JP）　⑪ 特許出願公開

⑫ 公開特許公報（A）　昭60－80193

㉛Int.Cl.⁴　識別記号　庁内整理番号　㊸公開　昭和60年(1985) 5月8日
G 11 C　7/00　6549－5B

審査請求　未請求　発明の数　1　（全5頁）

㊹発明の名称　メモリシステム

㉑特　願　昭58－186919
㉒出　願　昭58(1983)10月7日

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明　細　書

発明の名称　メモリシステム

特許請求の範囲

1．動作時間の異なる複数の記憶装置ブロックと、システムアドレス信号を受けて上記記憶装置ブロックに対するアクセスを検出するアドレスデコーダと、このアドレスデコーダの出力信号によって対応する記憶装置ブロックにおけるアクセス時間に相当する初期値が設定され、所定のパルス信号により時間計測動作を行う計数回路と、この計数回路の出力信号により記憶装置ブロックに対する書込み又は読み出しの動作時間の設定を行うタイミング制御回路とを含むことを特徴とするメモリシステム。

2．上記計数回路は、シフトレジスタにより構成されるものであることを特徴とする特許請求の範囲第1項記載のメモリシステム。

3．上記タイミング制御回路は、読み出し出力信号をラッチ回路に取り込むタイミング信号と、中央処理装置に送出する動作終了信号とを形成するものであることを特徴とする特許請求の範囲第1又は第2項記載のメモリシステム。

発明の詳細な説明

（技術分野）

この発明は、メモリシステムに関するもので、例えば、高速記憶装置を用いた記憶装置ブロックと低速記憶装置を用いた記憶装置ブロックとにより構成されたメモリシステムのタイミング制御に有効な技術に関するものである。

（技術背景）

例えば、高速ＲＡＭ（ランダム・アクセス・メモリ）、低速ＲＡＭあるいはＲＯＭ（リード・オンリー・メモリ）のようにそれぞれの動作時間が異なる複数の記憶装置ブロックによって１つのメモリシステムを構成する場合、各記憶装置ブロック毎での動作時間が異なるものであるので、そのタイミング制御に次のような問題が生じる。単一のタイミングにより全記憶装置ブロックの制御を行うと、最も低速の記憶装置ブロックの動作タイミングによって全記憶装置ブロックが動作させら

れてしまう。一方、それぞれの記憶装置ブロックに対して個別にタイミング発生回路を設けることによって、それぞれを最適なタイミングのもとにアクセスしようとすると、タイミング制御回路が複雑になり、構成部品点数が増加するという問題が生じる。

〔発明の目的〕

この発明の目的は、簡単な構成により動作時間の異なる複数の記憶装置ブロックをそれぞれ最適なタイミングのもとにアクセスすることができるメモリシステムを提供することにある。

この発明の前記ならびにそのほかの目的と新規な特徴は、この明細書の記述および添付図面から明らかになるであろう。

〔発明の概要〕

本願において開示される発明のうち代表的なものの概要を簡単に説明すれば、下記の通りである。すなわち、システムアドレス信号を受けて動作時間の異なる記憶装置ブロックに対するアクセスを検出し、この出力信号によって対応する記憶装置ブロックにおけるアクセス時間に相当する初期値が設定され、所定のパルス信号により時間計測動作を行う計数回路の出力信号により各記憶装置ブロックに対する書込み又は読み出しの動作時間の設定を行うようにするものである。

〔実施例〕

第１図には、この発明の一実施例のブロック図が示されている。この実施例のメモリシステムにおいては、特に制限されないが、高速記憶装置６と低速記憶装置７の２種類の記憶装置を用いた場合を例にして説明する。

この実施例では、次のようなタイミング制御回路によって上記記憶装置６，７のタイミング制御が行われる。すなわち、アドレスバスＡＢからのシステムアドレス信号を受けるアドレスデコーダ１によって上記２種類のメモリ装置６，７のいずれに対するアクセスかを検出する。この検出出力ｍ１，ｍ２は、セレクタ４の選択信号として利用される。このセレクタ４は、初期値Ｔ１，Ｔ２を保持している記憶手段２，３を選択して、シフトレジスタ５に初期値Ｔ１又はＴ２を供給する。シフトレジスタ５には、上記アドレスデコーダ１によって形成されたタイミング信号φ１により上記初期値Ｔ１又はＴ２がロードされる。特に制限されないが、このシフトレジスタ５は、１０ビットのシフトレジスタにより構成される。このシフトレジスタ５の第７ビットから第１０ビット目の出力信号Ｄ７～Ｄ１０が次のＡＮＤゲート回路Ｇ１～Ｇ４によって構成されたタイミング検出回路に供給される。

すなわち、第７ビット目の信号Ｄ７は、インバータ回路ＩＶ１によって反転され、第８ビット目の信号Ｄ８とともにＡＮＤゲート回路Ｇ４の入力に供給される。このＡＮＤゲート回路Ｇ４の出力信号は、記憶装置６又は７の読み出し出力信号D_{out}を受けるラッチレジスタ８のストローブ信号として使用される。上記アドレスデコーダ１の出力信号ｍ１とシフトレジスタ５の第８ビット目の信号Ｄ８とは、ＡＮＤゲート回路Ｇ２の入力に供給される。このＡＮＤゲート回路Ｇ２の出力信号ＣＳ１は、高速記憶装置６のチップ選択信号として使用される。上記アドレスデコーダ回路１の出力信号ｍ２とシフトレジスタ５の第８ビット目の信号Ｄ８とは、ＡＮＤゲート回路Ｇ３の入力に供給される。このＡＮＤゲート回路Ｇ３の出力信号ＣＳ２は、低速記憶装置７のチップ選択信号として使用される。また、シフトレジスタ５の第９ビット目の信号Ｄ９は、インバータ回路ＩＶ２により反転され、第１０ビット目の信号Ｄ１０とともにＡＮＤゲート回路Ｇ１の入力に供給される。このＡＮＤゲート回路Ｇ１の出力信号は、図示しない中央処理装置（ＣＰＵ）に送出する動作終了信号ＡＣＫとして使用される。

一方、上記タイミング制御回路によって制御される記憶装置側は、各記憶装置６，７のデータ入力D_{in}と上記ラッチレジスタ８を介したデータ出力D_{out}'とは、双方向バッファ９を介してデータバスＤＢに接続される。なお、各記憶装置６，７には、アドレスバスＡＢからのアドレス信号が供給されるものである（図示せず）。

次に、この実施例のメモリシステムの動作を第2図及び第3図のタイミング図に従って説明する。

第2図には、低速記憶装置7（M2）に対してアクセスを行った場合のタイミング図が示されている。この実施例では、特に制限されないが、その初期値T2として0111111100が記憶手段3に保持されている。したがって、記憶装置7を選択するようなシステムアドレス信号がアドレスデコーダ1に供給されると、その出力信号m2が形成されてセレクタ4を介して上記初期値T2がシフトレジスタ5に供給される。そして、この出力信号m2とクロックφとで形成されたロード信号φ1に同期して、上記初期値T2がシフトレジスタ5に取り込まれる。したがって、第1個目のクロックφのタイミングでは、第7，8ビット目の信号D7，D8とが1となり、残り第9，10ビット目の信号D9，D10は0となる。このような初期値T2は、クロックφに従って順次1ビットづつ右側にシフトされる。このシフト動作により1クロックづつ遅れて信号D9，D10が順次1になる。また、7個目のクロックφが到来したとき、初期値T2における第1ビット目の0が第7ビット目にシフトされてくるので信号D7が0になる。以後、1クロックづつ遅れて信号D8～D10も順次0に変化する。

以上のシフトレジスタ5のシフト動作により、上記アドレスデコーダ1の出力信号m2の選択信号（論理"1"）と、上記第8ビット目の信号D8を受けるANDゲート回路G3の出力信号CS2により記憶装置7（M2）が選択状態にされる。そして、信号D7が0（ロウレベル）に変化するとき、ストローブ信号φ2が形成されるので、読み出し動作であれば記憶装置7からの読み出し信号Doutがラッチレジスタ8に取り込まれる。さらに、2クロック分遅れて信号D9が0になるので、ANDゲート回路G1により動作終了信号ACKが送出されてそのアクセスが終了する。すなわち、図示しない中央処理装置CPUは、上記動作終了信号ACKを受けて、上記読み出されたデータDout'を双方向バッファを介して受け取るものである。なお、書込み動作であれば、上記チップ選択期間CS2の間に入力データDinを記憶装置7に供給し、上記同様な動作終了信号ACKの転送を待って動作を終了させるものである。

第3図には、高速記憶装置6（M1）に対してアクセスを行った場合のタイミング図が示されている。この実施例では、特に制限されないが、その初期値T1として0000011100が記憶手段2に保存されている。したがって、記憶装置6を選択するようなシステムアドレス信号がアドレスデコーダ1に供給されると、その出力信号m1が形成されてセレクタ4を介して上記初期値T1がシフトレジスタ5に供給される。そして、この出力信号m1とクロックφとで形成されたロード信号φ1に同期して、上記初期値T1がシフトレジスタ5に取り込まれる。したがって、第1個目のクロックφのタイミングでは、第7，8ビット目の信号D7，D8とが1となり、残り第9，10ビット目の信号D9，D10は0となる。このような初期値T1は、クロックφに従って順次1ビットづつ右側にシフトされる。このシフト動作により1クロックづつ遅れて信号D9，D10が順次1になる。また、3個目のクロックφが到来したとき、初期値T1における第5ビット目の0が第7ビット目にシフトされてくるので信号D7が0になる。以後、1クロックづつ遅れて信号D8～D10も順次0に変化する。

以上のシフトレジスタ5のシフト動作により、上記アドレスデコーダ回路1の出力信号m1の選択信号（論理"1"）と、上記第8ビット目の信号D8を受けるANDゲート回路G3の出力信号CS1により記憶装置6（M1）が選択状態にされる。そして、信号D7が0（ロウレベル）に変化するとき、ストローブ信号φ2が形成されるので、読み出し動作であれば記憶装置6からの読み出し信号Doutがラッチレジスタ8に取り込まれる。さらに、2クロック分遅れて信号D9が0になるので、ANDゲート回路G1により動作終了信号ACKが送出されてそのアクセスが終了する。すなわち、図示しない中央処理装置CPUは、上

記動作終了信号ACKを受けて、上記読み出されたデータD_{out}'を双方向バッファを介して受け取るものである。なお、書込み動作であれば、上記チップ選択期間CS1の間に入力データD_{in}を記憶装置6に供給し、上記同様な動作終了信号ACKの伝送を待って動作を終了させるものである。

以上の動作により、低速記憶装置7は、クロックφが7個分の期間動作状態にされ、高速記憶装置6は、クロックφが3個分の期間動作状態にされる。したがって、この実施例では、上記クロックφの1周期とクロックの数とによりメモリ装置の動作時間と一致させるものである。このような動作時間（アクセスタイム）の設定は、上記初期値の設定により簡単に実現できるものである。

（効　果）

(1)アドレスデコーダ、シフトレジスタ、セレクタ及びゲート回路のような簡単に回路により構成された単一のタイミング制御回路によって、その動作時間の異なる複数の記憶装置からなり、各記憶装置の動作時間に応じたサイクルのもとに動作させることができるメモリシステムを得ることができるという効果が得られる。

(2)上記(1)により簡単な回路によりタイミング制御を行うことができるから、メモリシステム全体の故障率を減少させることができるという効果が得られる。

(3)上記(1)によりタイミング制御回路の構成部品点数が少なくてすむから、低価格のメモリシステムを得ることができるという効果が得られる。

(4)上記(1)により、各記憶装置を最適動作サイクルでアクセスすることができるから、メモリアクセス時間に無駄が生じない。したがって、記憶情報の入出力を合理的に行うことができるという効果が得られる。

以上本発明者によってなされた発明を実施例に基づき具体的に説明したが、この発明は上記実施例に限定されるものではなく、その要旨を逸脱しない範囲で種々変更可能であることはいうまでもない。例えば、3種類以上の記憶装置に対しては、上記初期値を保持する記憶手段と、ゲート回路を追加することによって上記同様にそれぞれの動作時間に応じたタイミング制御を行うことができる。また、各記憶装置の動作時間に応じた時間設定を行う回路は、上記シフトレジスタに代えプログラマブルカウンタ等のような時間計測（パルス計数）回路を用いるものであってもよい。

さらに、各回路ブロックの具体的回路の構成は、種々の実施形態を採ることができるものである。

（利用分野）

この発明は、動作時間の異なる複数の記憶装置からなるメモリシステムに広く利用できるものである。

図面の簡単な説明

第1図は、この発明に係るメモリシステムの一実施例を示すブロック図、

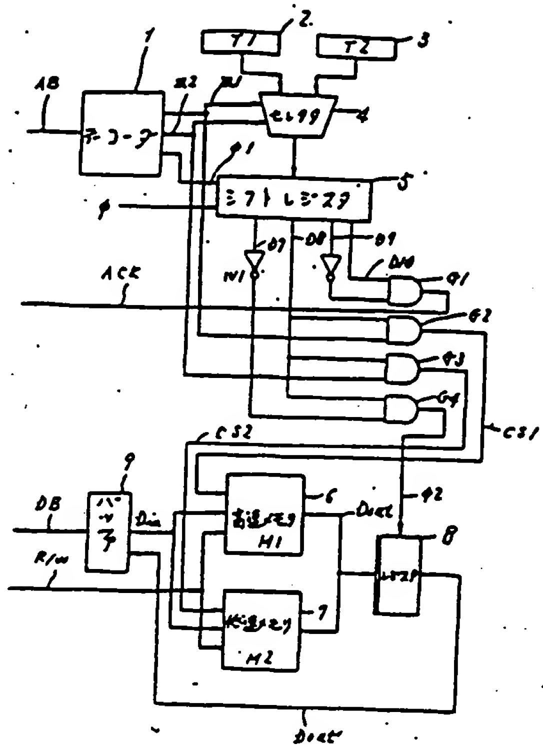
第2図は、低速記憶装置のタイミング制御を説明するためのタイミング図、

第3図は、高速記憶装置のタイミング制御を説明するためのタイミング図である。

1・・アドレスデコーダ、2，3・・記憶手段、4・・セレクタ、5・・シフトレジスタ、6・・高速記憶装置、7・・低速記憶装置、8・・ラッチレジスタ、9・・双方向バッファ

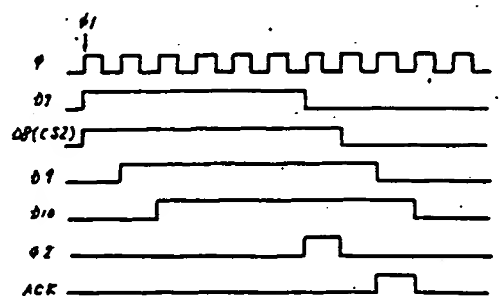
代理人弁理士　高橋　明夫

第 1 図



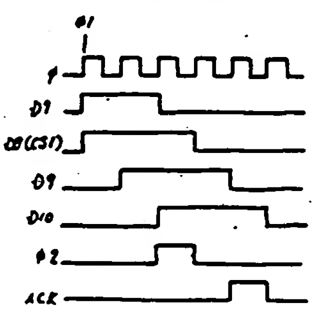
1
2
3
4
5
6
7
8
9
T1
T2
AB
ACK
DB
R/W
φ
φ1
φ2
D7
D8
D9
D10
N1
G1
G2
G3
G4
CS1
CS2
Din
Dout
M1
M2

第 2 図



φ1
φ
D7
D8(CS2)
D9
D10
φ2
ACK

第 3 図



φ1
φ
D7
D8(CS1)
D9
D10
φ2
ACK